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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/638,026	08/14/2000	Paul A. Farrar	M4065.0082/P082-A	8833

24998 7590 03/26/2002

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EXAMINER	
PAREKH, NITIN	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action in Ex Parte Reexamination	Control No. 09/638,026	Patent Under Reexamination FARRAR, PAUL A.	
	Examiner Nitin Parekh	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

a☒ Responsive to the communication(s) filed on *28 December 2001* . b☒ This action is made FINAL.
c☐ A statement under 37 CFR 1.530 has not been received from the patent owner.

A shortened statutory period for response to this action is set to expire 3 month(s) from the mailing date of this letter. Failure to respond within the period for response will result in termination of the proceeding and issuance of an *ex parte* reexamination certificate in accordance with this action. 37 CFR 1.550(d). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).** If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☐ Information Disclosure Statement, PTO-1449.
3. ☐ Interview Summary, PTO-474.
4. ☐ _____.

Part II SUMMARY OF ACTION

1a. ☒ Claims *40-51 and 68-73* are subject to reexamination.
1b. ☐ Claims _____ are not subject to reexamination.
2. ☐ Claims _____ have been canceled in the present reexamination proceeding.
3. ☐ Claims _____ are patentable and/or confirmed.
4. ☒ Claims *40-51 and 68-73* are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ The drawings, filed on _____ are acceptable.
7. ☐ The proposed drawing correction, filed on _____ has been (7a)☐ approved (7b)☐ disapproved.
8. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
   a)☐ All b)☐ Some* c)☐ None of the certified copies have
   1☐ been received.
   2☐ not been received.
   3☐ been filed in Application No. _____ .
   4☐ been filed in reexamination Control No. _____.
   5☐ been received by the International Bureau in PCT application No. _____.
   * See the attached detailed Office action for a list of the certified copies not received.
9. ☐ Since the proceeding appears to be in condition for issuance of an *ex parte* reexamination certificate except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte* Quayle, 1935 C.D. 11, 453 O.G. 213.
10. ☐ Other: _____

cc: Requester (if third party requester)

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 40-51, 68-72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US Pat. 5925931) in view of Akram (US Pat. 5808360) and the admitted prior art (APA).

Regarding claims 40-51, 71 and 72, Yamamoto discloses a semiconductor device comprising:

- a semiconductor structure having a metal contact (23 in Fig. 7) formed on the surface thereof
- a first insulator layer (24/41 in Fig. 7) overlying the metal contact
- a metal pad/interconnection (50 in Fig. 7) overlying the first insulator layer and in contact with the metal contact, the metal pad being partially overtop of the metal contact
- a second insulator layer (47 in Fig. 7) overlying the metal pad
- the metal contact being connected to the metal pad by a via hole (25/42 in Fig. 7) in the first insulator, and

- Solder contact/ball (48 in Fig. 7) formed in the second insulator layer and in contact with the metal pad, the solder contact/ball extending from the top of the second insulator layer to the metal pad by a through-hole formed in the second insulator (Fig. 7)

(Fig. 7; Col. 6, line 40- Col. 7, line 5; Col. 4-8).

Yamamoto fails to specify the diameter of the solder contact/ball being less than 100, 50, 25, 10 microns or being approximately 2 microns.

The APA discloses using conventional 100 microns diameter solder balls in C4 bonding of an integrated circuit/wafer to a substrate such as module or circuit board.

Akram teaches using solder microbumps having a diameter ranging from 15-100 microns (30 in Fig. 1C; Col. 5, line 7- 32) in a flip chip interconnection. Akram further teaches using the microbumps having mushroom/hemispherical shaped top/tip portion where the total height (Fig. 1C and 3) is in the range of 1-60 microns and the diameter of the microbumps being smaller than the pad dimension (Col. 5, line 1-16). The Fig. 1C and 3 of Akram show the dimensions and the relative comparison of the total height and diameter of the microbumps and pad dimension. It would be obvious to a person of ordinary skill in the art to realize that the microbumps can have the diameter in a range of 1-60 microns.

Furthermore, the selection of parameters such as size and shape of the solder contacts including diameter, pitch/spacing, pad dimension, thickness of an insulating layer, etc. in chip packaging and interconnection technology art is a matter of design choice to achieve the desired I/O density, performance and reliability.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to select the solder contacts having diameter less than 100, 50, 25, 10 or approximately 2 microns to achieve the desired connection density and performance using Akram's microbump configuration in Yamamoto's device. microns to achieve the desired connection density and performance using Akram's microbump configuration in Yamamoto's device.

Regarding claim 68, Yamamoto discloses the first insulating layer being 10-50 microns thick (Col. 4, line 39) but fails to specify the first insulating layer being 2 microns thicker than the metal contact. However, it can be clearly seen in Fig. 7 of Yamamoto's device that the first insulating layer (41/24 in Fig. 7; Col. 4, line 39)) is 2-3 times thicker than the metal pad which is conventionally approximately 10 microns thick (see Akram, Col. 4, line 18).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first insulating layer being 2 microns thicker than the metal contact to achieve desired degree of protection/passivation in Yamamoto's device in view of Akram and APA.

Regarding claims 69 and 70, Yamamoto further discloses the metal pad/interconnection comprising a stack of four different metals comprising Zinc, Nickel, Copper, Gold (43/44/45/46A/46B/50 in Fig. 7; Col. 5, line 9-35) but fails to specify using Zirconium as one of the four metals. It is conventional in the chip packaging and interconnection technology art to use metals such as Nickel, Copper, Gold, Zirconium, Palladium, etc. in forming metal pad/interconnection.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the metal pad comprising a stack of four different metal levels comprising Zirconium, Nickel, Copper and Gold to achieve the desired electrical properties passivation in Yamamoto's device in view of Akram and APA.

3. Claim 73 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US Pat. 5925931) in view of Akram (US Pat. 5808360) and the admitted prior art (APA).

Applicant's claim 73 do not distinguish over Yamamoto in view of Akram and the admitted prior art (APA) regardless of the process used to form the solder contacts/bumps, because only the final product is relevant, not the process of making such as "exposing the resist or removing/etching ". Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177

USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Response to Arguments

4. Applicant's arguments filed on 12-28-02 have been fully considered but they are not persuasive.

A. Applicant contends that the combination of Yamamoto, Akram and APA is not proper since they involve different technologies/processes.

However, as explained above, Yamamoto discloses a structure using solder balls/contacts for an interconnection of a chip to a substrate. Akram teaches a structure using the solder microbumps/contacts to achieve the interconnection of a chip to a substrate. The structures in APA, Yamamoto and Akram use solder balls/contacts to achieve the desired interconnection. Therefore, Akram's teaching related to the dimensions of the solder contacts is applied to Yamamoto and APA's device structure to

achieve the desired dimensions of the solder contacts in the claimed structure regardless of the process/method used to form the solder contacts.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NP
March 20, 2002

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800